What is claimed is:

Sub A7

1. An A/D converter, comprising:

a plurality of capacitors and at least one comparator, arranged to form an analog to digital conversion of an analog input signal to a digital output signal; and

a control circuit, controlling said capacitors to be used for both analog to digital conversion and for calibration.

2. A converter as in claim 1, wherein said control circuit controls a level which is supplied to said capacitors.

3. A converter as in claim 1, further comprising a plurality of level latches, storing levels associated with calibration, and connected to control respective levels applied to said capacitors.

4. A converter as in claim 2, wherein said control circuit controls a level which is supplied to a bottom plate of each said capacitor, and wherein a top plate of each said capacitor is connected together to form a common line.

5. A converter as in claim 2, further comprising an image acquisition element, obtaining information indicative of a

portion of an image, and producing an output indicative thereof, said an output being analog to digitally converted by said analog to digital converter.

6. A converter as in claim 4, wherein said level supplied to a bottom plate of each said capacitors can be one of two different voltage levels or a ground level.

7. A converter as in claim 4, wherein said level applied to a bottom plate of each capacitor can be a first voltage level which is double a value of said first voltage level.

8. A converter as in claim 5, wherein said image acquisition element is a MOS element.

9. A converter as in claim 8, wherein said image acquisition element is one of a MOS photo diode or a MOS photo gate, and forms an active pixel sensor.

10. A converter as in claim 1, wherein said control circuit includes a latch, latching a level which is supplied to a bottom plate of each of a plurality of capacitors.

11. A converter as in claim 10, wherein said level can be one of ground or one of two voltage levels.

12. A converter as in claim 10, wherein said level can be one of ground or a single voltage level.

13. A converter as in claim 12, further comprising a plurality of level latches, respectively storing levels associated with calibration, and connected to control a level applied to said capacitors.

14. A converter as in claim 13, wherein said level latches store a negative version of a calibration level.

15. A converter as in claim 14, wherein said negative version is a two's compliment.

16. An A/D converter comprising:

a plurality of capacitors, each associated with a specified bit of the digital signal, and each having a top plate connected to a common line and a bottom plate, and a comparator, connected to receive said common line as an output of said capacitor at one input, and a signal at another input; and

a plurality of value latches, each storing a value, and each associated with one of said plurality of capacitors, and changing a value applied to said bottom plate of said capacitor.

17. A converter as in claim 16, wherein said latches store either a one or a zero, and apply either a ground level or a reference level to said capacitor bottom plates depending on the value stored by said latches.

18. A converter as in claim 16, further comprising a control circuit, controlling said value latches to store a calibration value, and use said calibration value during converting.

19. A converter as in claim 18, wherein the same said capacitors are used both for calibration and for A/D conversion.

20. A converter as in claim 17, wherein said reference level includes two reference levels, one higher than the other.

21. A converter as in claim 17, wherein said reference level includes a single reference level.

22. A converter as in claim 17, further comprising a switch, controlled by a level in said latch, and selectively providing either a ground level or a reference level to said capacitor.

23. A converter as in claim 18, further comprising an image sensing element, producing an output signal indicative of a portion of said image, said output signal being coupled to said plurality of capacitors and comparator to be A/D converted thereby.

24. A converter as in claim 23, wherein said image sensing element is an element formed in MOS.

25. A converter as in claim 23, wherein said image sensing element is an active pixel sensor, having a photoreceptor, a follower associated with said photoreceptor, and a selector which allows electronic selection, also associated with said photoreceptor.

26. A converter as in claim 25, wherein said image sensing element is one of a photo diode or a photo gate.

27. A converter as in claim 25, wherein said follower and said selector are each formed using CMOS.

28. A converter as in claim 27, wherein said value latches are each formed using CMOS.

29. A converter as in claim 28, wherein said value latches, said comparator and said capacitors, and a plurality of said image sensing elements, are each formed on a common substrate.

30. A converter as in claim 18, wherein said value latches are formed of CMOS.

31. A converter as in claim 18, wherein said value latches store a value calibration value.

32. A converter as in claim 18, wherein said value latches store a negative of a calibration value.

33. A method, comprising:

calibrating an A/D converter using first capacitors;

obtaining a signal to be converted by said A/D converter; and

converting said signal to digital using at least a plurality of said first capacitors for said converting.

34. A method as in claim 33, further comprising obtaining values associated with said calibrating, and storing said values in a memory.

35. A method as in claim 34, wherein said memory includes a plurality of bits associated with said capacitors, each bit storing a value which adjusts a level that is applied to each said capacitor.

36. A method as in claim 35, wherein said level is applied to a bottom plate of said capacitor, and a conversion is carried out using a top plate of said capacitor.

37. A method as in claim 33, further comprising applying a calibration level to at least one of said capacitors.

38. A method as in claim 33, further comprising storing a calibration level obtained during said calibrating, and using the stored calibration level to apply a calibration level to at least one of said capacitors based on a level of said calibration.

39. A method as in claim 38, wherein said level includes a single reference level and a ground level.

40. A method as in claim 38, wherein said level includes two different reference levels and a ground level.

41. A method as in claim 33, further comprising obtaining a signal indicative of a portion of an image, and using said signal for said converting.

42. A method as in claim 41, wherein said obtaining a signal comprises attaining a signal on the same substrate as said A/D converter.

43. A method as in claim 34, wherein said values include values directly obtained from said calibrating.

44. A method as in claim 34, wherein said values include complements of values obtained during said calibrating.

45. A method as in claim 33, wherein said calibrating further comprising obtaining a complement of a calibration level and storing said complement in a plurality of latch elements.

46. A method as in claim 33, further comprising storing a level associated with said calibrating in a plurality of latch elements, associating each of said latch elements with one of said first capacitors, and using said values to adjust a level on said capacitors according to a calibration level, during obtaining a signal.

47. A method, comprising:

obtaining a value indicative of calibration of an A/D converter using a plurality of capacitors to obtain said value;

storing said value in a latch associated with the A/D converter; and

converting an input value using said plurality of capacitors, and using said value stored in said latch.

48. A method as in claim 47, wherein said value stored in said latch is a multiple bit value, and associating its of said value stored in the latch with individual ones of said plurality of capacitors.

49. A method as in claim 48, further comprising using said value stored in said us a value of said capacitor.

50. A method as in claim 48, further comprising using said value to adjust a level applied to a bottom plate of said capacitor.

51. A method as in claim 47, wherein said input value is a value indicative of a portion of an image.

52. An active pixel sensor, comprising:

a semiconductor substrate, having a plurality of items formed thereon, said items including:

an image acquisition element, formed using MOS formation technology, and having an MOS follower associated therewith and an MOS selection transistor associated therewith, said image acquisition element producing an output signal indicative thereof; and

an A/D converter element, also formed using MOS formation technology, including a plurality of capacitors and a comparator, said plurality of capacitors operating both to calibrate said A/D converter element and to convert signals applied to said A/D converter element, the same capacitors being used both for said calibrate and for said converter, and further comprising a latch, having a plurality of digital storage portions, each formed of CMOS, and each storing a value based on

said calibrate, said values used for allowing said A/D converter to acquire signals.

53. A sensor as in claim 52, wherein said A/D converter is a successive approximation A/D converter.